A 1-V 2.4-GHz PLL Synthesizer with a Fully Differential Prescaler and a Low-Off-Leakage Charge Pump

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Abstract — **A 1-V 2.4-GHz-band fully monolithic PLL synthesizer was fabricated on 0.2-μm CMOS/SOI process technology. It includes a voltage controlled oscillator (VCO) and a 3-GHz fully differential dual-modulus prescaler on a chip. A low-off-leakage-current charge pump is used for open-loop FSK modulation. When the PLL is open loop mode, the frequency drift of the output is lower than 2.5 Hz/μsec. The output phase noise is –104 dBc/Hz at 1-MHz offset frequency. The power consumption of the PLL-IC core is 17 mW at 1-V supply voltage.**

I. Introduction

Mobile communication terminals have come into widespread use around the world, and the measures towards the construction of ubiquitous network society are being initiated. Such a network society needs communication terminals that consume less power and are less expensive than conventional one. One of the most effective ways of reducing power is minimize the supply voltage. We are developing 1-V RF components. We have already proposed a 1-V 2-GHz fully-integrated image-rejection receiver [1] and a 0.6-V voltage reference circuit [2]. The PLL synthesizer is one of most important components of an RF transceiver. It is used for the local oscillator and the FSK modulator. Fully monolithic PLL synthesizers have already been reported [3][4]. However, their lowest supply voltage is 1.5 V [4]. On the other hand, other RF components operating on a 1 V supply have been reported [1][5]. That is to say, the low-voltage design of PLL synthesizers has not improved compared with that of other RF components. This is probably because operating the prescaler at high speed and keeping constant output current of the charge pump in wide output voltage range is difficult at low supply voltage. In this paper, we describe a 1-V 2.4 GHz-band PLL synthesizer fabricated in fully depleted 0.2μm-CMOS/SOI process technology. The synthesizer chip include a voltage controlled oscillator (VCO) and a 3-GHz fully differential prescaler. A low-off-leakage-current charge pump is used for open-loop FSK modulation, its frequency drift is lower than 2.5 Hz/μsec. The power consumption of a PLL-IC core is 17 mW at 1-V supply voltage.

II. Circuits Design

The proposed PLL is an integer-N-type PLL comprising a reference divider, phase frequency detector, charge pump, VCO, and programmable divider. The loop filter is not on the chip. The programmable divider is a pulse-swallow type and composed of a dual modulus prescaler and two CMOS counters. A modified tuning-range switching technique [6][7] is applied to the VCO because it keeps wide frequency range under low-supply-voltage. A schematic of the VCO is shown in Fig. 1. The VCO is a CMOS balance type and has 3 NMOS varactors. Two of these are for fine and course frequency control and the other one is for frequency modulation.

The fully differential dual-modulus prescaler is applied to the PLL. Because, the differential circuit architecture has advantages with single-end architecture especially under low supply voltage. When the supply voltage is lowered, the amplitude of the signal has to be small. Therefore, the noise and DC offset margins of the signal become small. On the other hand, the signal amplitude of the fully differential method is two times bigger than that of the single-end method. Therefore, the noise and DC offset margin of the signal become high. Figure 2 shows a block diagram of the fully differential prescaler. This circuit features feedback paths, FF2 to FF1 and FF3 to FF1, which both become differential signal. These feedback paths decide the maximum operating frequency of the dual modulus prescaler. Therefore, making them deferential is very effective for increasing maximum operating frequency. This circuit is composed of a newly designed current-mode fully differential OR/NOR gate and a conventional D-FF. The schematic of the OR/NOR gate and D-FF is shown in Fig. 3(a). The circuit has a three-transistor stack between VDD to GND. However, the body bias effect of transistors in fully depleted CMOS/SOI is very small, so the transistors in these circuit can switch. The conventional dual-modulus prescaler uses a D-FF with NOR gate as shown in Fig. 3(b). The data inputs of this D-FF with NOR gate are single phase. Therefore, the feedback paths of the conventional dual-modulus prescaler

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are single phase. However, applying the current-mode fully differential OR/NOR gate makes the feedback paths differential.

A charge pump uses the low-off-leakage technique. Figure 4 shows the schematic of the low-off-leakage charge pump circuit. One of the easiest ways to achieve FSK modulation is to input modulation data directly to the VCO. In this instance, the PLL must be able to change to the open loop mode. The VCO control voltage is hold by capacitor of the loop-filter at the open loop mode. This is realized by changing the output of the charge pump to high impedance. The conventional way of realizing this is to turn off transistors M1 and M2. However, when a low-threshold voltage process suitable for low voltage is used, the VCO control voltage cannot be held, because the off-leakage current of the transistors in the low-threshold process is large. A low-off-leakage charge pump is formed by inserting a CMOS switch between drain of transistors M1 and M2 to the charge pump output. When the PLL is set to open loop mode, this switch turns off and transistors M1 and M2 turn on. In this state, the same current flows to transistors M1 and M2, and the impedance from point A to the output is much bigger than the impedance to M1 and M2. Therefore, the leakage current flowing to the output becomes very small. According to the simulation, it is possible to reduce the leakage current of an output by about 4 figures by the proposal method. Furthermore, a depletion-mode transistor is applied as the current source transistor to keep constant output current in wide output voltage range under low-supply voltage. The channel regions of the depletion-mode transistors are undoped, which means they can be fabricated without additional process steps.

III. Experimental Results

Figure 5 shows a photograph of the PLL chip. The active area is about 1 mm x 1.5mm. The chip was fabricated in fully depleted 0.2-μm-CMOS/SOI process technology. Figure 6 shows the measurement result of the prescaler TEG. The maximum operating frequency was 3.4 GHz and supply current was 11.5 mA at 1-V supply voltage and input signal level of –20 dBm. Figure 7 shows the phase noise at the output frequency of 2.44 GHz. The loop bandwidth was designed to be about 10 kHz. The phase noise was about –104 dBc/Hz at 1-MHz offset frequency. The phase noise specification of Bluetooth are included in Fig. 6 for reference [8]. Figure 8 shows the transient characteristics of the PLL. The graph shows the frequency step response from 2.34 GHz to 2.44 GHz at 0 sec. The PLL changed to open-loop mode at 1 msec, and a modulation data was input at 2 msec. These data indicate that a frequency switching time was shorter than 600 μsec in this loop design and that the frequency drift is lower than 2.5 Hz/μsec. In this experiment, a hold capacitance was 2.2 nF and the frequency conversion gain of the VCO was about 500 MHz/V. Therefore, the off-leakage current of the charge pump will be calculated to be lower than 11 pA. This drift rate has fully meets the Bluetooth specification [8]. The power consumption of the PLL-IC core is 17 mW, whiches 11.5 mW for the prescaler and 4 mW for the VCO, at a 1-V supply voltage. The characteristics of the PLL are summarized in Table I.

Table. I

Chip Size (Active area)	1.0 mm x 1.5 mm
Phase Noise	> -104 dBc/Hz @ 1MHz
Frequency Switching Time	> 600 μsec
Frequency Drift Rate	2.5 Hz/μsec
Current Consumption Prescale	11.5 mA
VCO	4 mA
Other	1.5 mA
Total	17 mA
Supply Voltage	1V

III. CONCLUSIONS

A 1-V 2-GHz-band CMOS monolithic PLL using a fully differential dual-modulus prescaler and a low off-leakage change pump has been proposed. The PLL is suitable for low supply voltage and achieves low power consumption. We fabricated the PLL on 0.2-um CMOS/SOI process technology. The phase noise is about –104 dBc/Hz at 1-MHz offset frequency. The frequency drift is lower than 2.5 Hz/μsec, when a PLL is in the open-loop mode. Therefore, it can be used for the local oscillator as well as the FSK modulator of the 2.4-GHz ISM band wireless terminals. The PLL will reduce the cost, size, and power consumption of wireless terminals.

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[8] Specification of the Bluetooth System.

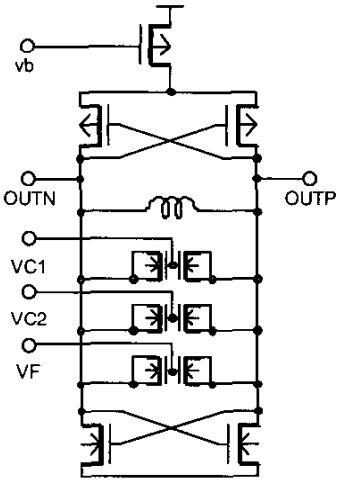


Fig. 1 Schematic of the VCO

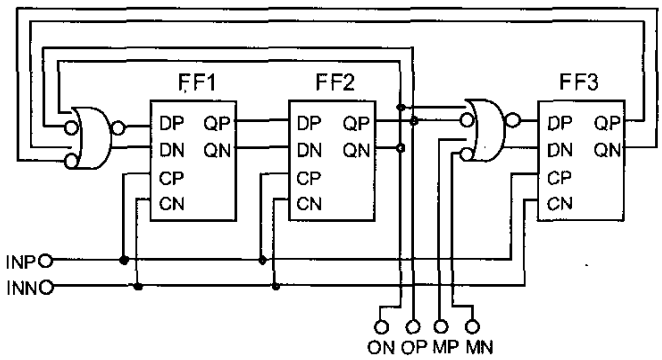
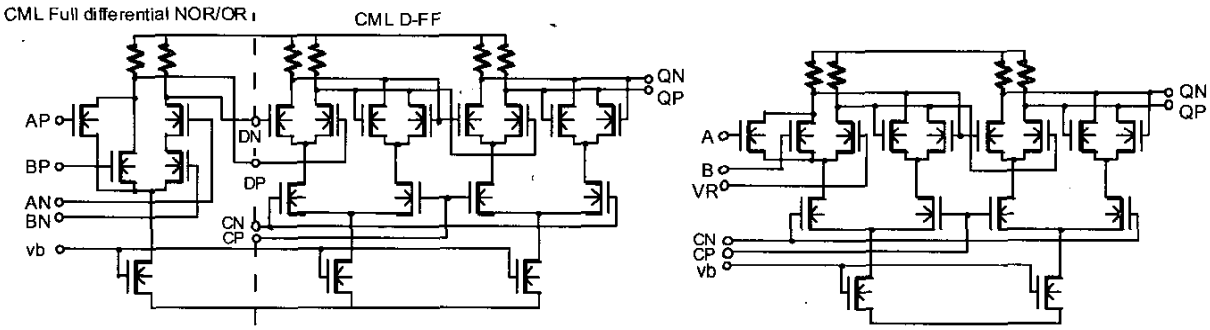


Fig. 2 A full differential 4/5 prescaler block diagram



(a) (b)

Fig. 3 Schematic of the D-FF with NOR gate.

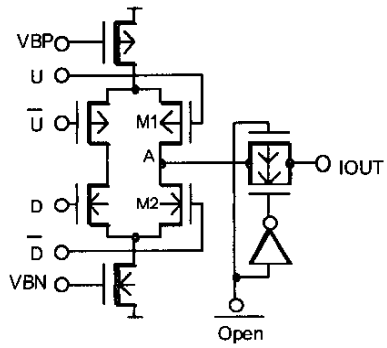


Fig. 4 Schematic of the low off-leakage charge pump.

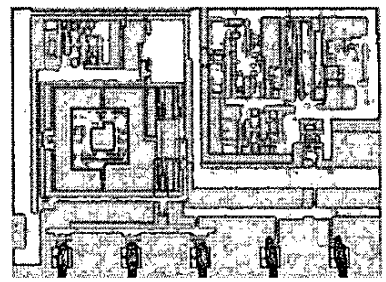


Fig. 5 Photograph of the PLL chip.

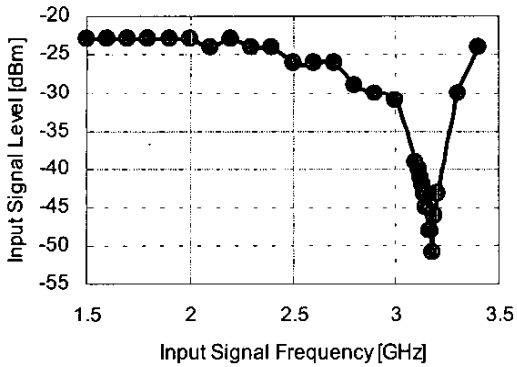


Fig. 6. Input sensitivity of the prescaler (33 divide mode).

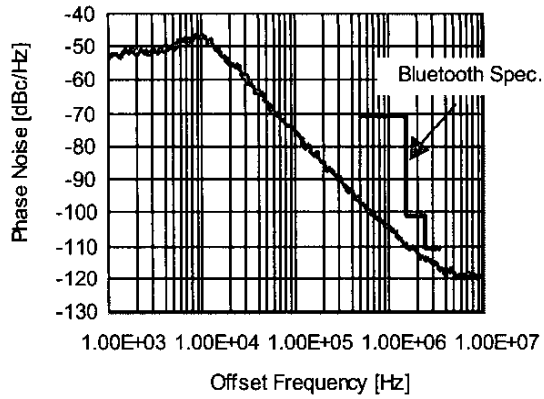


Fig. 7 Phase noise performance.

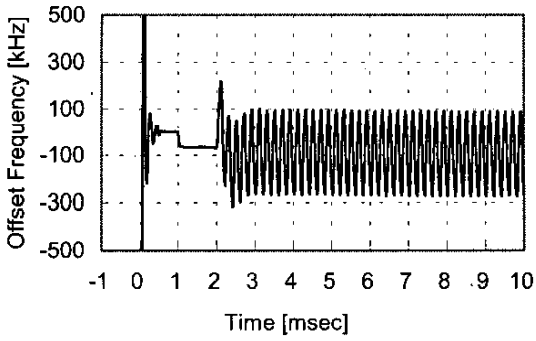


Fig. 8 Transient characteristics of the PLL.